Efficiency Estimation of Iterative Control System Design Method: Theoretical and Experimental Aspects

Yury V. Kolokolov, Andrey P. Sholonik, Pavel S. Ustinov and Abdelaziz Hamzaoui

Abstract—**In this paper theoretical and experimental aspects of an estimation of a design method efficiency of pulse energy converter (PEC) control systems are presented. The key idea of the proposed method is an iterative application of stage of classical frequency domain design, based on small signal modeling, with a consecutive nonlinear dynamics analysis. This method application and experimental confirmation is demonstrated on an example of control system design of direct current-direct current (DC-DC) buck converter.**

I. Introduction

In the majority of practical cases the required effective and safe mode of the pulse energy converter (PEC) operation represents an energy conversion stable process with the switching frequency f_{SW}. This operation mode is often called as a fundamental one (1*T*-mode ($T = 1/f_{SW}$)), all other operation modes (subharmonic, quasiperiodic and chaotic) are considered to be undesirable. Realization of the operating mode strictly depends on results of the control system design. The fundamental mode would be realized in the PEC, if design process was successful, otherwise one of the undesirable modes would be realized.

The basic design problem is to determine how specific parameter values influence the PEC performance specifications (overshoot, settling time and steady-state error). Basing on this information, control system parameters are selected so that all design specifications are satisfied. While this process is sometimes straightforward, more often than not it involves many design iterations, since control system parameters usually interact with each other and influence design specifications in conflicting ways [1].

The control system analysis and design method, based on PEC frequency responses, is used in the most majority of practical applications [2]. Frequency responses are plotted with help of transfer functions, which, in turn, were derived by small signal modeling [3, 4]. This design method is widespread in engineer practice because of its simplicity and efficiency. However, there are following shortcomings, inherent to this method:

- small signal model is adequate only in the presence of small state variable perturbations in the neighbourhood of steady-state operating point;
- it is impossible to predict an appearance of some undesirable dynamic modes [5, 6];
- there is an uncertainty in choice of the switching frequency (f_{SW}) to PEC open-loop crossover frequency (f_{CR}) ratio. The value of f_{SW}/f_{CR} is recommended to select within range 4÷10 [7], 3÷10 [8] or 10÷15 [9] in accordance with the rule-of-thumb. It is not clear also what value should be chosen in every specific case. It has been noted only that the value of f_{SW}/f_{CR} decrease leads to probability increase of the undesirable dynamic mode appearance [9]. The value of f_{SW}/f_{CR} increase leads to probability decrease of undesirable dynamic mode appearance and is not considered to be an effective decision, because it can result in the designed PEC performance specification degradation (increase of overshoot, settling time and steady-state error). It should be mentioned that, if equivalent small signal model is stable, this fact will not guarantee an undesirable dynamics absence in the designed PEC [5, 6], especially, when the value of f_{SW}/f_{CR} is minimum.

There are not many papers, presented as formalized design guidelines or handbooks, which can be useful in engineering practice, in spite of presence of a great number publications in the field of nonlinear dynamics in switching power converters (for example, see [10-14]).

This paper belongs to the area of practical importance and is considered to be a prolongation and generalization of the previous author works [15, 16]. The paper represents an attempt at application of the bifurcation theory instrument to the PEC control system design. The design method consists of two main stages: *the stage of control system design in the frequency domain* and *stage of nonlinear dynamics analysis*. Control system design, based on small signal modeling in the frequency domain, is realized at the first stage; control system dynamics investigation and estimation of performance specifications, based on nonlinear model, is realized at the second stage.

The paper is organized as follows. In section 2 the brief description of design method is presented. In section 3 a mathematical model is composed. In section 4 an example of the proposed method application for the control system design of the DC-DC buck converter is discussed. In section 5 a procedure of an experimental verification is presented.

Yu. V. Kolokolov and A. P. Sholonik are with Department of Design and Technology of Electronic and Computer Systems, Orel State Technical University, 29 Naugorskoye Shosse, 302020 Orel, Russia (e-mail: 2kolo@mail.ru, sholonik@yandex.ru).

P. S. Ustinov is with Department of Design and Technology of Electronic and Computer Systems, Orel State Technical University, 29 Naugorskoye Shosse, 302020 Orel, Russia and CReSTIC, Université de Reims Champagne-Ardenne, Moulin de la Housse, BP 1039, 51687 Reims Cédex 2, France (e-mail: pavel-ustinov@yandex.ru).

A. Hamzaoui is with CReSTIC, Université de Reims Champagne-Ardenne, Moulin de la Housse, BP 1039, 51687 Reims Cédex 2, France (e-mail: abdelaziz.hamzaoui@univ-reims.fr).

II. DESIGN METHOD BRIEF DESCRIPTION

The proposed method is presented in a form of an algorithm and consists of sequential iterations, each of them includes three stages. Only main points of design method are presented in this section, more detailed discussion concerning the proposed method one can find in [15, 16].

The first stage. Control system design, based on the small signal models [3, 4], in the frequency domain.

The second stage. Dynamics analysis of the PEC with the designed control system in some domain **Pn** of a parameter space **P** with an application of Poincaré stroboscopic mapping is

$$\mathbf{X_n} = \mathbf{F}(\mathbf{X_{n-1}}), \quad (1)$$

where $\mathbf{X_{n-1}}$ and $\mathbf{X_n}$ is a state variable vector at the time moments $t_{n-1} = (n-1)\cdot T$ and $t_n = n \cdot T$ accordingly; T is a pulse width modulation (PWM) period; $n \in \mathbb{N}$ is a PWM period number; **F(·)** is a vector function that sets a relationship between state variable vector at the time moments $t_{n-1} = (n-1)\cdot T$ and $t_n = n \cdot T$ accordingly.

As it was above-mentioned, only the fundamental dynamic mode (1*T*-mode) is required within whole parameter variation domain. Therefore, the fundamental mode stability is investigated at every point of the domain **Pn** of the parameter space **P**. The equation for state variable vector of the fundamental mode determination follows from equation (1) and has a form

$$\mathbf{F}(\mathbf{X}^*) - \mathbf{X}^* = 0, \quad (2)$$

where $\mathbf{X}^*$ is a state variable vector of the fundamental mode.

Stability is estimated with application of Jacoby matrix eigenvalues (multipliers) that can be determined from equation

$$\det(\mathbf{J} - \rho_i \mathbf{E}) = 0, \quad (3)$$

where $\mathbf{J} = \left.\frac{\partial \mathbf{F}}{\partial \mathbf{X}}\right|_{\mathbf{X}=\mathbf{X}^*}$ is a Jacoby matrix; **E** is a unit matrix; ρ_i are Jacoby matrix eigenvalues ($i = \overline{1,n}$, $n = rank(\mathbf{X}^*)$).

Absolute value of maximum multiplier is denoted as

$$\rho = \max|\rho_i|. \quad (4)$$

If $\rho < 1$, then dynamic mode will be stable.

The third stage. Correction of the original data (e.g., by means of ratio of f_{SW}/f_{CR} change) according to results of the algorithm second stage and step to the next design iteration or an exit from algorithm.

The main idea of the algorithm is to improve the PEC performance and to exclude undesirable dynamic modes from dynamics of the PEC by means of ratio of f_{SW}/f_{CR} iterative change, beginning from some starting value. This starting value should be chosen within generalized (3; 15) range that recommended in [7, 8, 9]. The value of L_{END} depends on the PEC performance required.

Control system design in the frequency domain takes place at the first algorithm iteration for some value of f_{SW}/f_{CR} (e.g., $f_{SW}/f_{CR} = 15$). After that, the model (1) is derived for the designed PEC control system. The model (1) is investigated at the specific set of points that belong to the domain **Pn** of the parameter space **P**. PEC functional peculiarities and possible change of the PEC parameter values determine the investigating domain **Pn**. The main goal of the investigation is to detect the presence (or absence) of the undesirable dynamic modes. The fundamental mode ($\mathbf{X}^*$) determination by means of equation (2) solve and Jacoby matrix eigenvalues estimation are realized at every point of the domain **Pn**. The PEC functional peculiarities determine the quantity of the parameters that should be varied and steps of both parameter and ratio of f_{SW}/f_{CR} variation. Comparison of performance specifications of the control system, designed at the current iteration, with the required specifications takes place at the analysis stage also besides evaluation of the fundamental mode stability.

After that, if eigenvalues $\rho < 1$ and performance specifications do not correspond to required ones for all investigated points of the domain **Pn**, then the value of f_{SW}/f_{CR} decreases and transition to the second iteration is carried out. If undesirable dynamics ($\rho > 1$) is revealed or $\rho < 1$, but performance specifications are satisfied, at the first iteration, then algorithm stops. If the algorithm stopped because of satisfaction of an inequality $\rho > 1$, then it would be possible to exclude the undesirable dynamics by means of an increase of the initial ratio of f_{SW}/f_{CR} and to carry out the algorithm again, but control system performance will degrade as a result in this case. A change of the control system structure and consecutive algorithm application is also acceptable.

The above-mentioned sequence is repeated within the second iteration. If ρ is more than unit or performance specifications correspond to required ones at any point of the domain **Pn**, this process stops. The return to the previous value of f_{SW}/f_{CR} and designed control system parameter values occurs, if $\rho > 1$. This is an exit from the algorithm.

III. MATHEMATICAL MODEL

A. *Nonlinear mathematical model of power stage*

An equivalent circuit of the DC-DC buck converter is shown in Fig. 1.

The equivalent circuit consists of two parts (Fig. 1): power stage and control system. The control process is realized by means of different control law (P, PI, PD, PID) application and PWM.

The parameter values of the equivalent circuit (Fig. 1) were the following: $R_L = 0.27\ \Omega$ is an ESR of the output filter inductor; $R_C = 0.18\ \Omega$ is an ESR of the output filter capacitor; $L = 890\ \mu H$ is an output filter inductor; $C = 170\ \mu F$ is an output filter capacitor; $\beta_U = 0.25$ is an

output voltage sensor gain; $U_0 = 2.5$ V is a magnitude of a sawtooth voltage; $U_{ref} = 3$ V is a reference voltage; $f_{SW} = 24$ kHz is a frequency of PWM. An input voltage E varies within the range $E = (20 - 28)$ V during investigation, a load resistance — within the range $R_{load} = (6 - 15)$ Ω. Design in the frequency domain was realized for $E = 24$ V and $R_{load} = 10$ Ω.

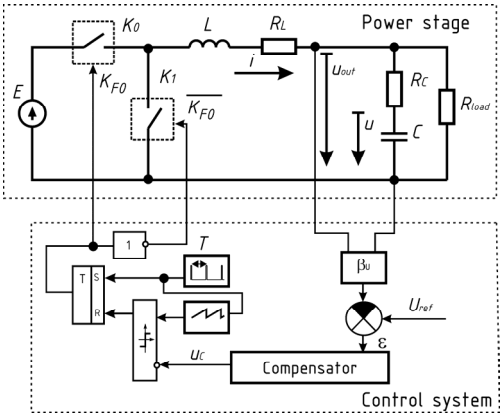

Fig. 1. Equivalent circuit of DC-DC buck converter

A nonlinear mathematical model of a power stage has a form of the second order vector ordinary differential equation with the discontinuous right-hand side:

$$\frac{d\mathbf{X_{PS}}(\gamma)}{d\gamma} = T \cdot \mathbf{A_{PS}} \cdot \mathbf{X_{PS}}(\gamma) + T \cdot \left(\mathbf{B_{PS1}} \cdot K_{F0} + \mathbf{B_{PS0}}\left(1 - K_{F0}\right)\right), \tag{5}$$

where $\mathbf{X}(\gamma) = \left(i(\gamma),\ u(\gamma)\right)^{\mathrm{T}}$ is a power stage state variable vector; $i(\gamma)$ is an output filter inductor current; $u(\gamma)$ is an output filter capacitor voltage; $\gamma = \frac{t}{T}$, $\gamma \in [0,1]$ is a duty ratio;

$$\mathbf{A_{PS}} = \begin{pmatrix} \frac{-1}{L}\left(R_L + \frac{R_C R_{load}}{R_C + R_{load}}\right) & \frac{-1}{L}\frac{R_{load}}{R_C + R_{load}} \\ \frac{1}{C}\frac{R_{load}}{R_C + R_{load}} & \frac{-1}{C}\frac{1}{R_C + R_{load}} \end{pmatrix}, \quad \mathbf{B_{PS1}} = \begin{pmatrix} \frac{E}{L} \\ 0 \end{pmatrix},$$

$\mathbf{B_{PS0}} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}$ are matrix and column vectors, defined by the element values of the converter equivalent circuit power stage (Fig. 1).

The switching function K_{F0} in the model (5) is calculated according to the algorithm

$$K_{F0} = \begin{cases} 1, & 0 < \gamma \le \gamma_0; \\ 0, & \gamma_0 < \gamma \le 1, \end{cases} \tag{6}$$

where γ_0 is a switch moment, corresponding to the transition of switch K_0 to the non-conducting state and switch K_1 to the conducting state.

B. *Small signal model of power stage*

Design in the frequency domain is realized with the help of frequency responses derived on the base of small signal modeling [3, 4, 17]. Block diagram of the DC-DC buck converter is presented in the Fig. 2.

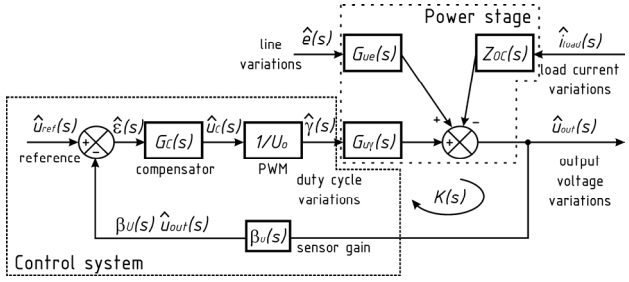

Fig. 2. Small signal block diagram of DC-DC buck converter

It is evident from Fig. 2 that an output voltage can be determined as

$$\hat{u}_{OUT} = G^{clos}_{u_{OUT}u_{ref}} \cdot \hat{u}_{ref} + G^{clos}_{u_{OUT}e} \cdot \hat{e} \pm Z^{clos}_{OC} \cdot \hat{i}_{load}, \tag{7}$$

where $G^{clos}_{u_{OUT}u_{ref}} = \frac{G_c G_{u\gamma}/U_0}{1 + \beta_U G_c G_{u\gamma}/U_0}$ is a closed-loop reference-to-output transfer function; $G^{clos}_{u_{OUT}e} = \frac{G_{ue}}{1 + \beta_U G_c G_{u\gamma}/U_0}$ is a closed-loop input-to-output transfer function; $Z^{clos}_{OC} = \frac{Z_{OC}}{1 + \beta_U G_c G_{u\gamma}/U_0}$ is a closed-loop output impedance; G_c is a compensator transfer function; $G_{u\gamma}$ is a power stage control-to-output transfer function; G_{ue} is a power stage input-to-output transfer function; U_0 is a sawtooth voltage amplitude; β_U is a sensor gain.

Equation (7) became:

$$\hat{u}_{OUT} = \frac{1}{\beta_U}\frac{K}{1+K} \cdot \hat{u}_{ref} + \frac{G_{ue}}{1+K} \cdot \hat{e} \pm \frac{Z_{OC}}{1+K} \cdot \hat{i}_{load}, \tag{8}$$

where $K(s) = \beta_U(s) G_c(s) G_{u\gamma}(s)/U_0$ is an open-loop voltage gain, which determines a stability of the closed-loop system by means of phase margin test.

The power stage control-to-output transfer function $G_{u\gamma}$ in the equation $K(s) = \beta_U(s) G_c(s) G_{u\gamma}(s)/U_0$ is defined as

$$G_{u\gamma}(s) = G_0 \cdot \frac{T_1 \cdot s + 1}{T_2^2 \cdot s^2 + 2\xi T_2 \cdot s + 1}, \tag{9}$$

where $G_0 = \frac{E \cdot R_{load}}{R_L + R_{load}}$ is a DC gain; $T_1 = R_C \cdot C$ and $T_2 = \sqrt{\frac{(R_C + R_{load}) \cdot C \cdot L}{R_L + R_{load}}}$ are the output filter time constants;

$\xi = \dfrac{((R_C + R_{load}) \cdot R_L + R_C R_{load}) \cdot C + L}{2\sqrt{(R_C + R_{load})(R_L + R_{load}) \cdot C \cdot L}}$ is the output filter damping factor.

Taking into the consideration that $G_c(s) = 1$, expression for $K(s)$ becomes:

$$K(s) = \frac{\beta_U(s)}{U_0} \cdot G_0 \cdot \frac{T_1 \cdot s + 1}{T_2^2 \cdot s^2 + 2\xi T_2 \cdot s + 1}. \quad (10)$$

With an application of Bode plots, constructed on the basis of transfer function (10), one can evaluate a stability of the PEC. The system has the phase margin $\Delta\varphi = 27°$ and the crossover frequency $f_{CR} = 1.3$ kHz, i.e. $f_{SW}/f_{CR} = 19$. Such quantity of phase margin ($\Delta\varphi = 27°$) is not sufficient to provide the PEC stability, that is why a compensating network must be introduced.

IV. Example of control system design for DC-DC buck converter

A. *Design stage with application of small signal model*

It is necessary to provide the phase margin value of (45-60)° [18] to provide the converter stability. The frequency ratio is recommended to select within range $f_{SW}/f_{CR} = 3 \div 15$ [7, 8, 9]. It is possible to increase the phase margin with application of PD lead-type compensating network. The equivalent circuit of this compensating network is depicted in Fig. 3.

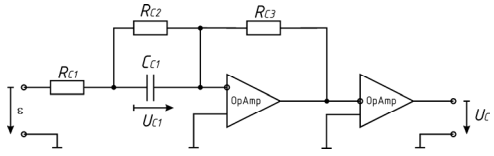

Fig. 3. PD lead-type compensating network equivalent circuit

The transfer function of the chosen compensating network (Fig. 3) becomes

$$W_C(s) = K_C \cdot \frac{T_{C1} \cdot s + 1}{T_{C2} \cdot s + 1}, \quad (11)$$

where $K_C = \dfrac{R_{C3}}{R_{C1} + R_{C2}}$ is a DC gain of the compensating network; $T_{C1} = R_{C2} \cdot C_{C1}$ and $T_{C2} = \dfrac{R_{C1} \cdot R_{C2} \cdot C_{C1}}{R_{C1} + R_{C2}}$ are the compensating network time constants.

The following values of the time constants were chosen to satisfy the stability requirements: $T_{C1} = 5.1 \cdot 10^{-5}$ s, $T_{C2} = 1.7 \cdot 10^{-5}$ s. The parameter values of the compensating network were the following: $R_{C1} = 0.5$ kΩ, $R_{C2} = 1$ kΩ, $R_{C3} = 15$ kΩ, $C_{C1} = 51$ nF.

The compensated system has the crossover frequency ($f_{CR} = 2.3$ kHz) and the phase margin $\Delta\varphi = 53°$. This is considered to be sufficient [18]. The frequency ratio equals 10.8 ($f_{SW}/f_{CR} = 10.8$) in this case. A transition to the second (analysis) stage of the algorithm takes place after the successful design in the frequency domain. Dynamics is investigated and performance specifications are evaluated at the analysis stage, but it is necessary to introduce some modifications to the mathematical model (5).

An equation describing a new state variable $u_{C1}(\gamma)$ (u_{C1} is a capacitor voltage of the compensating network) becomes:

$$\frac{du_{C1}(\gamma)}{d\gamma} = T \cdot \left(-\frac{\beta_U}{R_{C1}C_{C1}} \frac{R_C R_{load}}{R_C + R_{load}} \cdot i(\gamma) - \right.$$
$$\left. - \frac{\beta_U}{R_{C1}C_{C1}} \frac{R_{load}}{R_C + R_{load}} \cdot u(\gamma) - \frac{R_{C1} + R_{C2}}{R_{C1}C_{C1}R_{C2}} \cdot u_{C1}(\gamma) + \frac{U_{ref}}{R_{C1}C_{C1}} \right). \quad (12)$$

Therefore, after an introduction of the equation (12) and switching equation (13) into the system (5) one can derive the mathematical model, which describes an interaction of power stage and control system. The value of $\gamma_0 \in [0,1]$ is defined as the least root of the switching equation (13)

$$\zeta_0(\mathbf{X}(\gamma_0), \gamma_0) = \alpha \cdot (U_{ref} - \mathbf{S_0} \cdot \mathbf{X}(\gamma_0)) - U_0 \cdot \gamma_0 = 0, \quad (13)$$

where $\alpha = \dfrac{R_{C3}}{R_{C1}}$; $\mathbf{S_0} = \left(\beta_U \dfrac{R_C R_{load}}{R_C + R_{load}} \quad \beta_U \dfrac{R_{load}}{R_C + R_{load}} \quad 1 \right)$ is a row vector, converting state variable vector $\mathbf{X}(\gamma) = \left(i(\gamma), \; u(\gamma), \; u_{C1}(\gamma) \right)^{\mathrm{T}}$ to the equivalent voltage that, in turn, is compared with the reference voltage (U_{ref}).

The model (5) with the introduced additional equation (12) is linear on the intervals of the power stage structure constancy, so one can "sew" its solutions, taking into the consideration the fact that $\mathbf{X}(\gamma)$ vector depends on time continuously, and the resulting Poincaré mapping is

$$\mathbf{X_n} = \mathbf{V_0} \cdot \left[\mathbf{V_1} \cdot (\mathbf{X_{n-1}} + \mathbf{D_1}) - \mathbf{D_1} + \mathbf{D_0} \right] - \mathbf{D_0}, \quad (14)$$

where $\mathbf{V_0} = e^{\mathbf{A_{PS}} \cdot T \cdot (1 - \gamma_0)}$, $\mathbf{V_1} = e^{\mathbf{A_{PS}} \cdot T \cdot \gamma_0}$, $\mathbf{D_0} = \mathbf{A_{PS}^{-1}} \cdot \mathbf{B_{PS0}}$, $\mathbf{D_1} = \mathbf{A_{PS}^{-1}} \cdot \mathbf{B_{PS1}}$, $n \in \mathbb{N}$.

B. *Analysis stage with application of nonlinear model*

Dynamics is investigated in the "input voltage - load" parameter plane $(E, R_{load}) \subseteq \mathbf{P}$ ($\mathbf{P}$ is the parameter space of mathematical model (5)). The input voltage E varied within $E = (20 - 28)$ V range, the load resistance R_{load} — within $R_{load} = (6 - 15)$ Ω range. Steps of these parameter change were the following — 0.1 V and 0.5 Ω accordingly. All calculations are realized with an application of MATLAB™ system.

It is necessary to design control system with the settling time $t_S \le 600$ μs. Dynamics investigation at $f_{SW}/f_{CR} = 10.8$ did not reveal a presence of the undesirable

dynamic modes at the first algorithm iteration, the performance specifications did not correspond to required ones. That is why value of f_{SW}/f_{CR} was decreased according to the algorithm and the transition to the next iteration took place. The value of f_{SW}/f_{CR} change is realized by means of resistor R_{C3} variation with the step of 20 kΩ. The settling time values, corresponding to the different values of f_{SW}/f_{CR}, are summarized in Table I. The settling time t_S was calculated on the base of the nonlinear model (14). Transient response of the inductor current was modeled by the step-load change from 15 Ω to 6 Ω (in the design procedure only) and from 15 Ω to 12 Ω (as an additional test of the efficiency during an estimation of the performance specifications) for $E = 24$ V (nominal value). The transient response is considered to be faded, if the difference between an average value of the voltage (or current) and average steady-state value is less than 5 %.

TABLE I
PERFORMANCE SUMMARY (THEORETICAL)

iteration number	R_{C3}, kΩ	f_{SW}/f_{CR}	t_S, µs	
			15→6	15→12
1	15	10.8	700	350
2	***35***	***5.8***	***600***	***250***
3	55	3.7	500	200
4	75	2.6	400	150
5	95	2.0	350	120
6	115	1.6	350	50

The performance specifications were satisfied at the second iteration (see bold row in Table I). Since further decrease of f_{SW}/f_{CR} allows an improvement of the performance specifications, the authors propose not to stop the design procedure to demonstrate an efficiency of the proposed method. It is evident from Table I that increase of R_{C3} from 15 kΩ to 115 kΩ leads to the performance improvement, for instance, settling time decreased from 700 µs to 350 µs (for 15→6 step-load change) and from 350 µs to 50 µs (for 15→12 step-load change).

The designed control system possesses better performance in comparison with the one, which could be achieved using traditional design in the frequency domain, based on the small signal models.

V. EXPERIMENTAL VERIFICATION

The parameter values of an experimental plant are the same as used in mathematical modeling in section 3. An "electronic" switch on the base of MOSFET IRF540 was developed by authors for a step-load change. The switching time of this "electronic" switch is equal to the value less than 100 ns. A necessity of such device development is explained by the fact that the switching time of a conventional tumbler switch may vary up to 800 µs, and this time value is comparable with the investigating settling time of the buck converter transient response.

The diagrams of the inductor current transient responses, recovered from an experimental plant (Fig. 4), are depicted in Fig. 5 and Fig. 6. The approximate settling time values, received experimentally, are summarized in Table II.

TABLE II
PERFORMANCE SUMMARY (EXPERIMENTAL)

R_{C3}, kΩ	f_{SW}/f_{CR}	t_S, µs	
		15→6	15→12
15	10.8	720	360
115	1.6	360	80

It should be noted that the value of $f_{SW}/f_{CR} = 1.6$ is near two times less than the lower border of the range $f_{SW}/f_{CR} = 3 \div 15$, recommended by [7, 8, 9] during the design procedure.

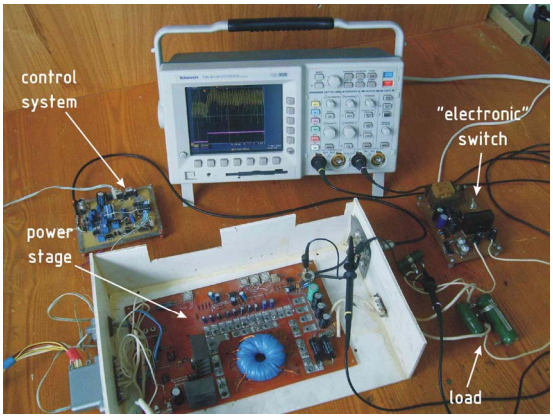

Fig. 4. Experimental plant

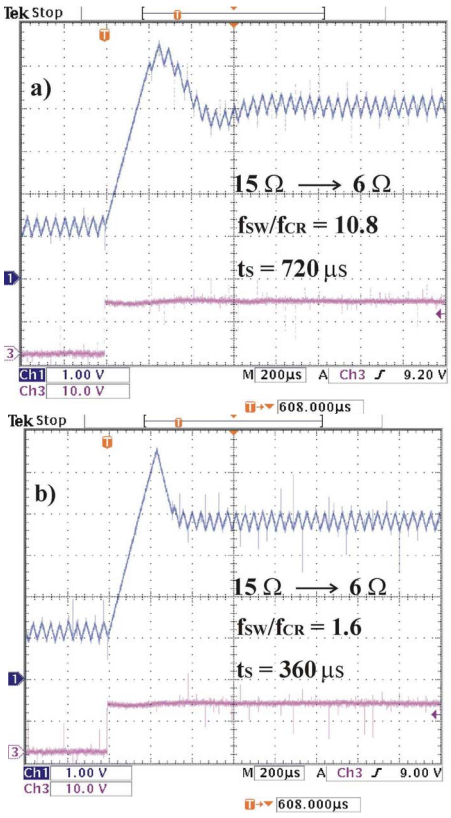

Fig. 5. Experimental step-load responses of inductor current (15 Ω → 6 Ω)

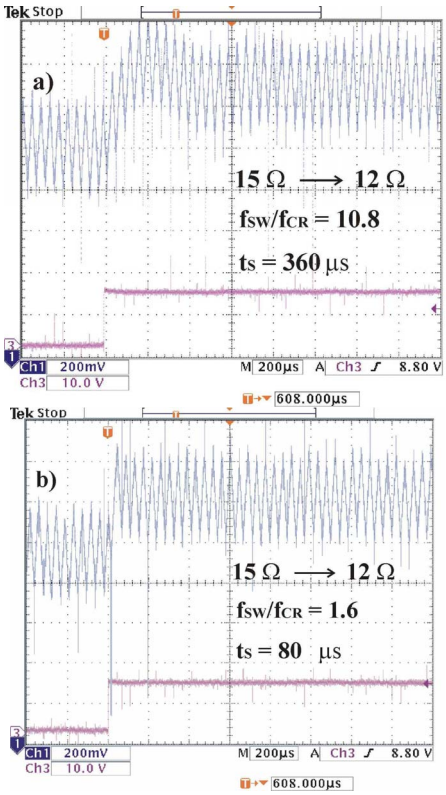

Fig. 6. Experimental step-load responses of inductor current (15 Ω → 12 Ω)

VI. Conclusions

The design method, presented in this paper, is a result of an investigation stage, carried out by the authors and devoted to the development of the modern PEC design methodology considering them as essentially nonlinear systems. This method combines simplicity of the frequency domain design with the opportunity of bifurcation phenomena revealing. In particular, it overcomes an uncertainty of switching frequency to PEC open-loop crossover frequency ratio choice and makes it possible to improve system performance. The iterative method efficiency was demonstrated theoretically (with the help of mathematical modeling) and experimentally on the example of control system design for the DC-DC buck converter. The result of the proposed method application: settling time was decreased in two times in comparison with the traditional frequency domain design.

References

[1] Kuo, B. C. & Golnaraghi, F. [2003] *Automatic control systems* (John Wiley & Sons, USA).

[2] Tse, C. K. & di Bernardo, M. [2002] "Complex behavior in switching power converters," Proc. of IEEE, Special Issue on Applications of Nonlinear Dynamics to Electronic and Information Engineering **90**(5), 768–781.

[3] Middlebrook, R. D. & Ćuk, S. [1976] "A general unified approach to modeling switching–converter power stages," *IEEE Power Electronics Specialists Conference*.

[4] Severns, R. & Bloom, G. [1985] *Modern dc-to-dc switchmode converter circuits* (Van Nostrand Reinhold Co, New York).

[5] Mazumder, S. K., Nayfeh, A. H. & Boroyevich, D. [2001] "Theoretical and experimental investigation of the fast- and slow-scale instabilities of a DC–DC converter," IEEE Trans. on Power Electronics **16**(2), 201–216.

[6] Mazumder, S. K. [2001] "Nonlinear analysis and control of standalone, parallel DC-DC, and parallel multi-phase PWM converters," PhD thesis, Virginia Polytechnic Institute and State University.

[7] Lehman, B. & Bass, R. M. [1996] "Switching frequency dependent averaged models for PWM DC-DC converters," IEEE Trans. on Power Electronics **11**(1), 89–98.

[8] Dixon, L. [2001] "Switching power supply control loop design," http://focus.ti.com/lit/ml/slup098/slup098.pdf.

[9] Meleshin, V. I. [2002] "Derivation of continuous linear model of the pulse converter power stage as an initial design phase of its dynamic properties," Elektrichestvo **10**, 38–43. (In Russian)

[10] Fossas, E. & Olivar, G. [1996] "Study of chaos in the buck converter," IEEE Trans. Circuits Syst. I **43**, 13–25.

[11] Yuan, G. H., Banerjee, S., Ott, E. & Yorke, J. A. [1998] "Border collision bifurcation in the buck converter," IEEE Trans. Circuits Syst. I **45**, 707–716.

[12] El Aroudi, A., Benadero, L., Toribio, E. & Olivar, G. [1999] "Hopf bifurcation and chaos from torus breakdown in a PWM voltage-controlled DC-DC boost converter," IEEE Trans. Circuits Syst. I **46**(11), 1374–1382.

[13] Zhusubaliyev, Zh. T., Soukhoterin, E. A., Rudakov, V. N., Kolokolov, Yu. V. & Mosekilde, E. [2001] "Bifurcations and chaotic oscillations in an automatic control relay system with hysteresis," Int. J. Bifurcation and Chaos **11**(5), 1193-1231.

[14] Dranga, O., Tse, C. K., Iu, H. H. C. & Nagy, I. [2003] "Bifurcation behavior of a power-factor-correction boost converter," Int. J. Bifurcation and Chaos **13**(10), 3107-3114.

[15] Kolokolov, Yu. V., Sholonik, A. P. & Ustinov, P. S. [2005] "Nonlinear controllers: a hybrid algorithm of synthesis," *2nd IEEE Int. Conf. "Physics and Control 2005"*, *PhysCon'2005*, August 24-26, St. Petersburg, Russia.

[16] Kolokolov, Yu. V., Sholonik, A. P., Ustinov, P. S., Hamzaoui, A. & Zaytoon, J. [2006] "Hybrid design method of nonlinear controllers: avoiding bifurcations," *IFAC Conf. on Analysis and Control of Chaotic Systems*, *CHAOS'06*, June 28-30, Reims, France.

[17] Erickson, R. W. & Maksimovic, D. [2001] *Fundamentals of power electronics* (Springer Science + Business Media Inc., USA).

[18] Banerjee, S. & Verghese, G. C., Eds. [2001] *Nonlinear phenomena in power electronics: attractors, bifurcations, chaos, and nonlinear control* (IEEE Press, New York).